IEEE RTSI 2018 – Track 2 – 3.9

POWER-AWARENESS AND RESOURCE MANAGEMENT IN MOBILE AND IOT COMPUTING SYSTEMS

Recently, multicore processors have become prevalent in the whole spectrum of computing systems, ranging from embedded solutions like mobile handheld devices to warehouse-scale systems like Google's datacenters. The growing amount of on-chip processing elements and their heterogeneity, coupled with the increasing number of concurrent applications, exponentially inflates the design-space of efficient computing systems calling for innovative performance- and power-aware resource management techniques. We need a deep rethinking of the hardware/software stack to manage the fundamental trade-offs between maximizing performance under a power cap. Computer architectures could leverage reconfigurable fabrics to dynamically specialize and support the performance/power requirements of fluctuating loads; compilers and runtimes should automatically tune code generation to better exploit the underlying computer architecture to reach the sweet-spot in terms of performance per Watt; operating systems should implement smart resource management techniques leveraging the dynamic knobs provided by both computer architectures (e.g., dynamic voltage and frequency scaling) and compilers (e.g., degree of parallelism). This session aims at gathering researchers from different research areas, from computer architecture to compilers/runtimes and operating systems, to present cutting edge research and discuss how to face this challenge.

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Short Curriculum Vitae

Donatella Sciuto received her Laurea in Electronic Engineering from Politecnico di Milano and her PhD in Electrical and Computer Engineering from the University of Colorado, Boulder. She is currently the Vice Rector Delegate of the Politecnico di Milano and a Full Professor at the Dipartimento di Elettronica e Informazione of the Politecnico di Milano, Italy. She is member IEEE, IFIP 10.5, EDAA. She is or has been member of different program committees of ACM and IEEE EDA conferences and workshops. Her main research interests cover the methodologies for the design of embedded systems and multicore systems, from the specification level down to the implementation of both the hardware and software components, including reconfigurable and adaptive systems. She has published over 200 papers.

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Short Curriculum Vitae

Simone Campanoni is a tenure-track assistant professor at the Electrical Engineering and Computer Science department of Northwestern University. Simone's main research areas are compilers and virtual machines, with special interest in computer architecture, runtime systems, operating systems, and programming languages. Simone addresses research challenges through vertical specialization of the hardware/software stack.
Simone started the HELIX research project at Harvard University in 2010 as a post-doc working with Profs. David Brooks and Gu-Yeon Wei. HELIX uses static and dynamic compilation, run-time optimization, and architecture specialization to extract coarse-grained parallelism for many-core architectures from complex "sequential" code.
Simone received his Ph.D. degree with highest honors from Politecnico di Milano University in 2009. His dissertation discusses theoretical and practical performance implications of thread level parallelism. To this end, Simone designed and built a bytecode virtual machine optimized for commodity multicore platforms. Simone is the author of ILDJIT, a parallel compilation framework that includes static and dynamic compilers as well as a bytecode virtual machine. ILDJIT has been used in several academic and industrial research projects, including HELIX.